

# Abstract

A battery cell charge/discharge and protection circuit and system employing enhancement-mode junction-gated transistors as gating switches and minimizing external components is disclosed. The use of an enhancement-mode switch device with a PN junction control gate enables the elimination of external or internal precision resistors through the compensation of the voltage drop across the switch with the forward drop across the PN junction for temperature invariance of switch channel current estimation. The use of variable current drive circuits combined with a capacitor connected to the gate of the switch device facilitates energy consumption optimization while providing a timing mechanism for determining the recovery duration after a fault condition. Elimination of precision resistors and the minimization of the capacitance value facilitate a low-cost, single-chip battery protection solution.

## Prior Art & References

1. Brown, Paul M. Jr.; US Patent 4,228,367, "*High speed integrated switching circuit for analog signals*", Issued: October 14, 1980
2. Zwanziger, Peter; US Patent 4,987,362, "*Self-regulating drive circuit for the base current of a power transistor with saturation level control*", Issued: January 22, 1991
3. Williams, Richard K.; US Patent 5,909,103, "*Safety switch for lithium ion battery*", Issued: June 1, 1999
4. Alwardi, Milad et. al.; US Patent 5,965,997, "*Battery monitoring circuit with storage of charge and discharge accumulation values accessible therefrom*", Issued: October 12, 1999
5. Morrill, David P.; US Patent 6,249,148, "*Low power variable base drive circuit*", Issued: June 19, 2001
6. MOXTEK <sup>TM</sup> Application Note "*Low Noise Junction Field Effect Transistors*", Feb. '01
7. Technology and product information for JFET devices from QSpeed Inc. (previously, Lovoltech Inc.) at the following URL: <http://www.qspeed.com/>